Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A vector processor for processing vector data comprising multiple element data using a register, the vector processor comprising:

a register usable as a vector register comprising multiple element registers; and

an addressing circuit for circularly specifying addresses of the vector register with the address of any element register of the vector register as the top.

2. (Original) The vector processor according to claim 1, wherein the resister is a set of multiple scalar registers, and, by any of the scalar registers being specified as the top, the addresses of the multiple scalar registers are circularly specified.

3. (Original) The vector processor according to claim 1, wherein the register comprises a vector register, any element register of the vector register being specifiable as the top.

4. (Currently Amended) The vector processor according to ~~any of claims 1 to 3,~~ claim 1, wherein, when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached.

5. (Currently Amended) The vector processor according to~~ any of claims 1 to 4,~~ claim 1, wherein, when writing the results of a vector operation to the register, element data of the

vector register are sequentially written to the addresses of the vector register beginning with the address specified as the top, and writing of the element data is continuable by returning to the top address if the end address is reached.

6. (Original) A register addressing method used for processing of vector data comprising multiple element data, wherein

a predetermined element register is treated as a vector register comprising multiple element registers, and, by specifying the address of any element register of the vector register as the top, the addresses of the element registers of the vector register are circularly specified.

7. (New) The vector processor according to claim 2, wherein, when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached.

8. (New) The vector processor according to claim 3, wherein, when performing a vector operation on data stored in the register, element data of the vector register are sequentially read from the addresses of the vector register beginning with the address specified as the top, and reading of the element data is continuable by returning to the top address if the end address is reached.

9. (New) The vector processor according to claim 2, wherein, when writing the results of a vector operation to the register, element data of the vector register are sequentially written to the addresses of the vector register beginning with the address specified as the top, and

writing of the element data is continuable by returning to the top address if the end address is reached.

10. (New) The vector processor according to claim 3, wherein, when writing the results of a vector operation to the register, element data of the vector register are sequentially written to the addresses of the vector register beginning with the address specified as the top, and writing of the element data is continuable by returning to the top address if the end address is reached.

11. (New) The vector processor according to claim 4, wherein, when writing the results of a vector operation to the register, element data of the vector register are sequentially written to the addresses of the vector register beginning with the address specified as the top, and writing of the element data is continuable by returning to the top address if the end address is reached.